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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,119	07/15/2003	Thomas Wiegele	015559-288	7843

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EXAMINER	
LIN, TINA M	
ART UNIT	**PAPER NUMBER**
2874	

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,119	WIEGELE ET AL.	
	Examiner	Art Unit	
	Tina M. Lin	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on May 9, 2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-68,72,74,80-86,88,89,91-94,96 and 98* is/are pending in the application.

4a) Of the above claim(s) *1-27 and 57-68, 72, 74, 80-86, 88, 89, 91-94, 96 and 98* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) in 4) are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/3/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's election without traverse of claims 28-56, drawn to a microstructure on a wafer in the reply filed on 09 May 2005 is acknowledged.

Drawings

The drawings are objected to because: The drawings filed with this application on 15 July 2003, are objected to as being informal. Notice that Figures 9-19 are hand drawn and the labels on the figures are handwritten. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 28, 29, 33, 37, 39-41, 43-48, 50-51 and 53-55 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,587,613 to De Natale.

In regards to claims 28, 39 and 41, De Natale discloses a wafer portion (Figure 7) including a microstructure (50) formed therein and located thereon and a solderable surface (Column 6) configured to receive an electrical component (66), there the solderable surface is electrically and operatively coupled to the microstructure so that if can control operate or receive inputs from at least part of the microstructure.

In regards to claims 29 and 33, De Natale discloses an upper wafer portion (50, 60, 70) and a lower wafer portion (92) where the microstructure (50) is located on the upper wafer portion and the solderable surface (solder pad) is located on the lower wafer portion. Furthermore, De Natale discloses the upper and lower wafer portions to be coupled together.

In regards to claims 37 and 40, De Natale discloses the solderable surface to be a flip chip connection site configured to receiver a chip thereon by flip chip bonding. (Column 6)

In regards to claim 43, De Natale discloses a microstructure with a sensor. De Natale further discloses the mirrors to be actuated, so therefore, an actuator must also be present in the microstructure.

In regards to claim 44, De Natale discloses a mirror array (52) including a plurality of movable reflective surfaces.

In regards to claim 45-47, De Natale discloses at least two electrodes (66) located below each of the reflective surfaces so that voltage applied across the electrodes and the reflective surfaces cause the reflective surfaces to move in at least two directions.

In regards to claim 48, De Natale discloses the reflective surfaces to be individually controllable. (Column 8)

In regards to claim 50, De Natale discloses an upper wafer portion (50, 60, 70) and a lower wafer portion (92) where the mirror array (52) (50) is located on the upper wafer portion and the solderable surface (solder pad) is located on the lower wafer portion. Furthermore, De Natale discloses the upper and lower wafer portions to be coupled together.

In regards to claim 51, De Natale discloses the reflective surfaces located on a silicon layer.

In regards to claim 53, De Natale discloses at least a portion of the upper wafer portion to be a SOI wafer.

In regards to claim 54, De Natale discloses a wafer portion to be a ceramic substrate.

In regards to claim 55, De Natale shows a lower wafer portion with an upper surface facing the upper wafer portion and the solderable surface located on the upper surface.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 30-32, 34-36, 38, 42, 49, 52 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,587,613 to De Natale.

In regards to claims 30-32, although De Natale does not explicitly state the upper or lower wafer portion to have a top view, it would have been obvious at the time the invention was made to a person having ordinary skill in the art that either the upper or lower wafer portion has a top view since the top view is dependant on the orientation of the device or the person. Therefore, the upper wafer portion would defines a coverage area in the top view and the solderable surface is not located within the coverage area, the upper wafer would include an outer perimeter where the outer perimeter defines the coverage area, and the lower wafer portion would have a coverage area in top view and wherein the coverage area of the upper wafer portion is entirely contained in the lower wafer portion.

In regards to claims 34-36, although De Natale does not explicitly state the upper and lower wafer portions to be coupled together by a low temperature or photopatternable adhesive. However. De Natale does not limit the coupling of the two wafer portions to soldering or flip chip bonding techniques. Furthermore, the use of adhesives is widely used technique to bond wafers and

substrates. Furthermore, when taking temperature/heat as a factor, the use of a low temperature adhesive would be preferable to prevent temperature from affecting other optical or electrical components. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have used a low temperature or photopatternable adhesive.

In regards to claim 38, De Natale discloses a plurality of conductive pads (82) each electrically isolated from any adjacent bad. But De Natale fails to disclose the conductive pads having a melting point of less than about 250°C. However, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have a melting point of less than about 250°C, since it has been held to be within the general skill of a worker in the art to select a known material or known characteristic on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416*

In regards to claims 42 and 49, De Natale fails to disclose a controller coupled to the solderable surface to cause and control the individual movement of each reflective surface. However, the use of a controller would have been obvious at the time the invention was made to a person having ordinary skill in order to determine how much voltage and current to input in order to position the movable mirrors to the proper placement at the appropriate time.

In regards to claim 52, De Natale fails to specifically disclose the reflective portions located on movable portions to be coupled to a base portion on the upper wafer. However, De Natale does disclose the mirrors/reflective portions to tip when actuated and therefore, when tipped, the mirrors are rotated. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have the moveable portions rotatably coupled to a base portion of the wafer.

In regards to claim 56, De Natale discloses a wafer portion (Figure 7) with an upper portion (50, 60, 70) and a lower portion (92) including a microstructure (50) formed therein and located thereon and a solderable surface (Column 6) configured to receive an electrical component (66), there the solderable surface is electrically and operatively coupled to the microstructure so that if can control operate or receive inputs from at least part of the microstructure. However, although De Natale does not explicitly state the upper or lower wafer portion to have a top view, it would have been obvious at the time the invention was made to a person having ordinary skill in the art that either the upper or lower wafer portion has a top view since the top view is dependant on the orientation of the device or the person. Therefore, the upper wafer portion would defines a coverage area in the top view and the solderable surface is not located within the coverage area, the upper wafer would include an outer perimeter where the outer perimeter defines the coverage area, and the lower wafer portion would have a coverage area in top view and wherein the coverage area of the upper wafer portion is entirely contained in the lower wafer portion.

The documents submitted by applicant in the Information Disclosure Statement have been considered and made of record. Note attached copy of form PTO-1449.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B-F all discuss wafer type structures with either MEMs mirrors or reflective mirrors controlled by electrical components.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made

in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tina M. Lin whose telephone number is (571) 272-2352. The examiner can normally be reached on Monday-Friday 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney Bovernick can be reached on (571) 272-2344. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TML

John D. Lee
Primary Examiner